REMARKS

The rejection of claims 2-11, 18-19, and 21 under 35 U.S.C. §103(a) as being unpatentable over Shimbo et al. (U.S. Patent No. 4,738,935) in view of Lee et al. (U.S. Patent No. 4,900,372) and Narayan et al. (U.S. Patent No. 5,208,182) is hereby traversed and reconsideration thereof is respectfully requested in view of the following remarks.

With regard to Shimbo et al., the Examiner states that "the bonded substrate of Shimbo et al. is composed of the identical materials in the specification and therefore optimization of these materials would have been anticipated to produce an expected result." The Applicants respectfully disagree with this statement, and assert that it is merely a potential aspect (i.e., composite substrate) of Applicants' invention that is disclosed by Shimbo et al, while claim 21, limitation (c), provides an interdependent relationship between this aspect (i.e., composite substrate) and other aspects (i.e., buffer layer, first epilayer) of the Applicants' invention, that neither Shimbo, nor the references, provide or disclose.

Shimbo et al. provide a method for manufacturing a compound semiconductor device wherein two compound semiconductor substrates having given impurity concentrations and thicknesses are bonded, thereby forming a junction with good electrical characteristics. Shimbo et al.'s method is irrespective of the lattice constant mismatch therebetween. Shimbo et al. do mention the difference in the thermal expansion coefficient between the first and second substrate (col. 3, lines 23-29) and, inconsistent with Applicants' claimed invention, provide a *preference* in the difference between the two substrate thermal expansion coefficients. Shimbo therefore does not provide a relationship such as presented by Applicants' independent claim 21, element (c), that includes an interdependent relationship between lattice constant and thermal expansion coefficients in selecting the materials, that parametizes the relationship between, firstly, the composite thermal expansion coefficient of a composite substrate formed from two compound semiconductor substrates, and the composite lattice constant and, secondly, a lattice constant of a buffer layer and a first epitaxial layer. Although Shimbo et al. may provide one combination for the composite substrate as disclosed by Applicants', it is the relationship as provided by limitation (c) of claim 21, that is neither

provided by Shimbo et al. alone, or as shall be established herein, in combination with Lee et al. and/or Narayan et al.

Particularly, the Examiner states that Shimbo et al. provide a bonded substrate of GaP/InP, which is also disclosed in claims 7-8 of the invention; however, as also provided by the Examiner, Shimbo et al. do not describe the so formed device for further fabrication (page 3, lines 1-3), and hence alone, do not provide for the limitations provided by Applicants' claim 21, element (c), that provides limitations based upon the second lattice constant and second thermal coefficient with respect to the first epilayer lattice constant's relationship to the composite lattice constant, and the buffer layer requirements as described therein.

Lee et al. provide a method for utilizing different annealing methods to balance stresses and produce decreased incidence of defects and thermal strain, however, Lee et al. do not provide any teachings according to Applicants' claim 21, element (c). Indeed, the one example provided by Lee et al. includes the growth of a GaAs epilayer on a GaAs buffer layer disposed on a SiGe substrate. Using this example, the criteria recited in claim 21, element (c) is not satisfied, and hence it is difficult to conceive how Lee et al. can be combined with Shambo et al. to provide the limitations of Applicants' claim 21.

Narayan et al. disclose a method of forming gallium arsenide on a silicon heterostructure including strained layer superlattices in combination with rapid thermal annealing to achieve a reduced threading dislocation density in the epilayers. Using an example from Narayan as applied to Applicants' invention, allow the Si layer and GaAs layer to be equivalent to the composite substrate of Applicants' invention, with a lattice constant between 5.43 Å and 5.65 Å, and a thermal expansion coefficient between 2.6 x 10^{-6} /°C and 6.9 x 10^{-6} /°C. Continuing the application of Narayan et al. to Applicants' claimed invention, allow the GaAs layer to be the first epilayer of the present invention. Like the example from Lee et al., the lattice constant of Narayan's epilayer is greater than the lattice constant of the composite substrate, while the thermal expansion coefficient of the epilayer is also greater than the thermal expansion coefficient of the composite. This is not consistent with the limitation of Applicants' claim 21, subsection (c), without even

considering the further limitations provided for the buffer layer of Applicants' invention. Narayan does not provide additional examples.

As Applicants show herein, the examples provided by Lee et al. and Narayan et al. do not conform to or otherwise demonstrate the limitations of Applicants' claim 21, limitation (c), alone, or in combination with each other and/or Shimbo et al.

Applicants agree with Examiner that it is well-known that optimizing thermal expansion properties and lattice constant properties is desirable, and that techniques such as composite substrates, annealing methods, and buffer layers are also well-known to attempt to achieve this objective, but it is the interdependent combination of first epilayer characteristics, second substrate layer characteristics, and buffer layer characteristics, as provided particularly by Applicants' claim 21, limitation (c), that provides a method that is novel and unobvious when compared to the prior art. The present invention is therefore not merely a recognition of the fact that parameters are to be optimized, but rather, Applicants' invention provides a methodology for optimization that is neither disclosed in the prior art nor applicable to the examples provided therein. Accordingly, Applicants disagree that the limitation of claim 21, element (c), are obtainable by routine experimentation.

Accordingly, Applicants respectfully submit that the subject matter disclosed in claim 21 of the present invention is novel and non-obvious over the prior art of record, and allowance is respectfully requested. All remaining claims depend from claim 21.

Based on the above Remarks, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this Response, the Examiner is invited to contact the undersigned at 617-832-1241.

Respectfully submitted,

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